Multicarrier Modem Core on FPGA

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Abstract— **The paper deals with the realization on FPGA of a filter bank based multicarrier modem core. The main blocks of the modem core are for the transmitter : OQAM modulation for transmitter, Synthesis Filter Bank composed from IFFT and Polyphase network; and for the receiver : OQAM modulation for receiver, Analysis Filter Bank composed from Polyphase network and FFT. The modem core is implemented on FPGA with 10^6 gates and its frequency is 7.34kHz per frame with 512 real data.**

INTRODUCTION

Multicarrier techniques are becoming more and more popular in communication systems. Orthogonal frequency division multiplexing (OFDM) technique attracts a lot of attention due to its efficient implementation using Fast Fourier Transform (FFT). However, in order to cope with a frequency selective channel, a cyclic prefix must be added leading to a spectral efficiency loss. As an alternative, filter bank based multicarrier modems avoid the need of guard interval between consecutive symbols [1]. Furthermore, they allow efficient sub-channel equalizers [2]. Consequently, they are good candidates for future multicarrier communication systems such as UMTS downlink or LAN. On the other hand, the progress in FPGA technology during the last years, especially programmable circuits with embedded multipliers, considerably increased the possibilities to integrate communication system-on-a-chip [3]. In [4] the authors have built a multicarrier modem using 4 DSPs. In order to decrease the surface area, the research was oriented towards FPGA realizations [5,6]. This paper presents an implementation of a filter bank based multicarrier modem core on FPGA and it is organized as follows. Next section is a review of the filter bank multicarrier system. Then the hardware implementation of the modem is presented. Finally simulation results are given.

FILTER BANK MULTICARRIER MODEM PRINCIPLE

A filter bank based multicarrier modem employs two filter banks : a synthesis filter bank (SFB) at the transmitter side and a analysis filter bank (AFB) at the receiver [5]. They are generated through uniform frequency shifts of a prototype filter. The structure of OQAM filter bank based multicarrier modem is given on Fig. 1. The blocks of synchronization and equalization are not presented in this figure. The interface blocks are not considered in the paper and the channel is assumed ideal.

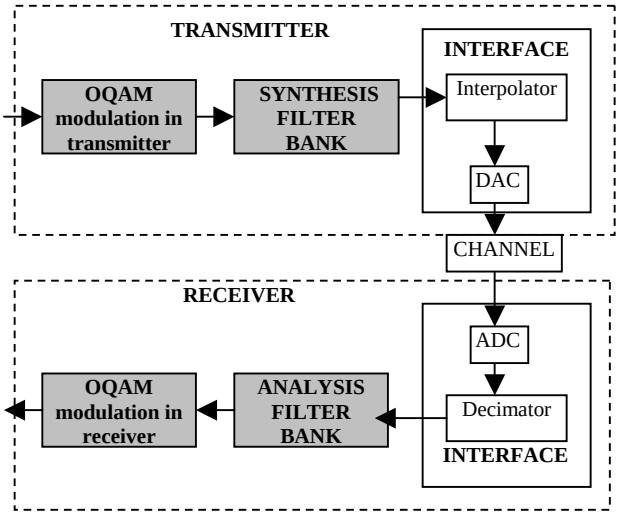
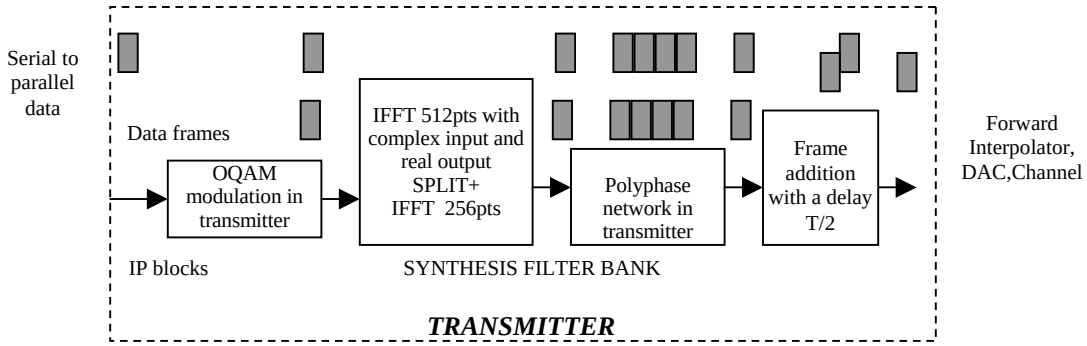


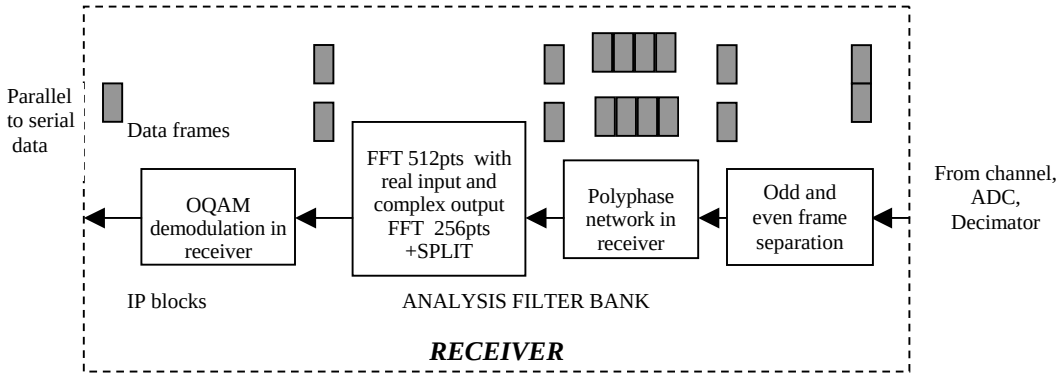
Figure 1. Filter bank based multicarrier modem

Like OFDM, the OQAM (Orthogonal Quadrature Amplitude Modulation) divides the transmission bandwidth into N subchannels with frequency spacing 1/T where T=2N/fsampling [7]. In OQAM modulation, the real and the imaginary part of the complex data symbols are alternatively transmitted at twice the conventional Nyquist rate. The imaginary part is delayed by T/2. Since the neighboring sub-channels overlap, it is necessary to apply the data alternatively to the real and imaginary sub-channels and in opposite manner for the two successive sub-channels (see table III). Therefore no guard interval is needed to cope with the impulse response of the channel.

The work described in this paper is partially supported from NATO grant PSL.CLG.977599/2005



2a. IP blocks and data frames in the transmitter



2b. IP blocks and data frames in the receiver

Figure 2. IP blocks and data frames in the filter bank multicarrier modem core.

ARCHITECTURE OF THE FILTER BANK MULTICARRIER MODEM CORE

The architecture of the modem is presented on Fig. 2. The IP blocks developed in VHDL are:

- *OQAM modulator IP in transmitter* – This IP block generates two frames, odd and even, with 256 complex data each from the initial frame which has 512 real data. The odd frame is generated from the first 256 data of the initial frame combined with zeros. The even frame is generated from the last 256 data of the initial frame combined with zeros. These two frames are processed separately in the IFFT and in the Synthesis filter bank. Then the odd and even frames are added in the Frame addition IP block with a delay of a half period T/2.
- *Frame addition IP* – This block keeps ½ frame out coming from the Synthesis filter bank at time index t-1 and adds it to the ½ frame outcoming from the SFB at time index t as shown at Fig. 3. It executes 256 addition of real data each T/2:

$$\begin{cases} Y_t(i)=Yodd_{t-1}(256+i)+Yeven_t(i) \\ Y_t(i+256)=Yodd_t(i)+Yeven_t(i+256) \end{cases}$$

$$1 \le i \le 256$$

The realization of the additions is serial.

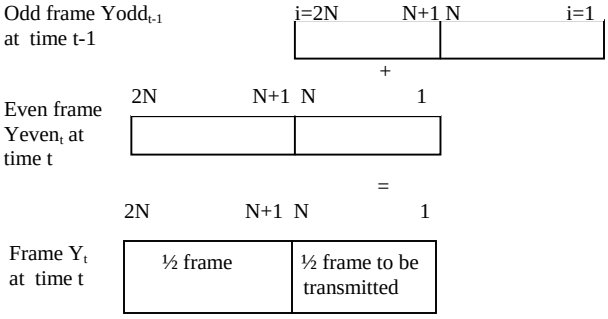


Figure 3. Frame addition IP in the transmitter with 2N=512

- *Frame separation IP* – This IP block separates odd and even frames in the receiver.
- *OQAM IP block in the receiver* – This IP block reconstructs the initial data frame with 512 real numbers from two consecutive blocks at the output of the FFT in the receiver. It takes the first 256 data from the odd frame and the next 256 data from the even frame.
- *Synthesis and Analysis filter banks IPs* - In a filter bank the filter prototype is half Nyquist. The polyphase network is obtained by the decomposition of low pass prototype FIR into 2N=512 sub-filters. Each sub-filter works at a cadence of 1/2N. A filter bank in the transmitter is composed from an IFFT followed by a

polyphase network and a filter bank in the receiver is composed by the polyphase network and the FFT.

- IFFT and the FFT IPs are with 512 points and have complex input data and real output data for the IFFT and real input data and complex output data for the FFT.

The Split function combined with 256 points IFFT/FFT replaces a 512 points IFFT with complex input and real output/FFT with real input and complex output.

The coefficients for the Split are calculated from the twiddle factors ω_{2N}^{i} of the IFFT/FFT with 2N=512 points as follows:

$$A(i) = \frac{1}{2}(1 - j\omega_{2N}^{i})$$

$$B(i) = \frac{1}{2}(1 + j\omega_{2N}^{i})$$

N=256, 2N=512, 1≤i≤256

There are 512 complex coefficients for the Split IP blocks.

The formulas for the Split for the IFFT are :

$$Y_R(i)=X_I(i)A_I(i)+X_R(i)A_R(i)+X_R(N-i)B_R(i)-X_I(N-i)B_I(i)$$

$$Y_I(i)=X_I(i)A_R(i)-X_R(i)A_I(i)-X_R(N-i)B_I(i)-X_I(N-i)B_R(i)$$

0≤i≤255 , X(256)=X(0)

The formulas for the Split for the FFT are :

$$X_R(i)=-Y_I(i)A_I(i)+Y_R(i)A_R(i)+Y_R(N-i)B_R(i)+Y_I(N-i)B_I(i)$$

$$X_I(i)=Y_I(i)A_R(i)+Y_R(i)A_I(i)+Y_R(N-i)B_I(i)-Y_I(N-i)B_R(i)$$

0≤i≤255 , Y(256)=Y(0)

The IP of the IFFT/FFT with 512 points integrates the Split processor with the butterfly processor, so that the Split is executed as the first stage in the IFFT and as the 8th stage in the FFT. The realization is serial with one multiplier-accumulator. The functions of 256 points IFFT/FFT consist in 7 stages with 128 butterfly processors each. They are realized serially with only one multiplier-accumulator.

- *Polyphase network IPs* – The Polyphase networks in the transmitter and in the receiver are realized with one IP block.

The prototype filter used in the transmitter and in the receiver is a FIR with 2047 coefficients. The second harmonic is 36dB inferior to the principle harmonic. The decomposition in 512 sub-filters with 4 coefficients, needs the addition of one null coefficient. The coefficients of the filter are:

$$h_{(1024+i)}=\frac{\cos\left(\pi\frac{i-1}{256}\right)}{\left(1-\left(\frac{i-1}{128}\right)^2\right)} \quad , \quad 1\le i\le 1024$$

$h_1=0$; $h_{129}=0$; $h_{1152}=\pi/4$;

$h_{(1024-i)}=h_{(1024+i)}$, 1≤i≤ 1023

The equation for the polyphase network in the transmitter is :

$$ys(i)=\sum_{k=0}^{3}h(i+kN)y_{2k}(i) \ , \quad i=1\le i\le 512$$

h(I+kN), i=1≤(i+kN)≤2048 – coefficients of the filter ;

$y_{2k}(i)$, 0≤k≤3, 1≤i≤512 – frames with 512 real data obtained from the IFFT at time index t, t-1, t-2, t-3

ys(i), i=1≤i≤512, frame outcoming from the Synthesis filter bank at time t. This frame is then added in the Frame addition IP block with the half frame from time t-1.

The equation for the polyphase network in the receiver is :

$$y_A(i)=\sum_{k=0}^{3}h(i+kN)y_{2k}(513-i) \ , \quad 1\le i\le 512$$

h(i+kN), 1≤(i+kN)≤2048 – coefficients of the filter ;

$y_{2k}(i)$, 0≤k≤3, 1≤i≤512 – frames with 512 real data coming from the Frame separator IP block in the receiver at times t, t-1, t-2, t-3

$y_A(i)$, 1≤i≤512, frame outcoming from the Polyphase network at time t and then entering in the FFT IP block.

All data in the modem core realization are coded on 16 bits 2's complement. Complex numbers contain real and imaginary parts coded on 16 bits 2's complement.

Results From Filter Bank Based Multicarrier Modem Core Implementation

In this realization priority was given to area minimization for a given minimal frequency per frame. All multiplications in the Filter Bank are executed serially and only one multiplier is used for the modem core.

The IP core is implemented on FPGA with 10^6 gates XC2V1000 from the VIRTEX II family of XILINX. All the simulations are executed using the ISE 6.1 development system [8]. The surface area and time characteristics of the filter bank multicarrier modem core are presented in Table I.

TABLE I. AREA AND TIME CHARACTERISTICS OF THE REALIZATION

IP block	BRAM	TBUF	MULT	Flip Flops	Slices	Clock cycles	Delay for f= 100MHz
OQAM Transmitter/ Receiver	1%	1%	-	1%	1%	2	20ns
FFT/IFFT +Split	22%	2%	2%	2%	6%	7168	72μs
Filter Bank	76%	2%	1%	2%	8%	6144	62μs
Frame Addition / Separation	1%	1%	-	1%	1%	2	20ns
Modem core	96%	6%	3%	6%	16%	13316	134μs

The processing time for a frame is 134μs. The modem frequency is 7.46kHz per frame.

TABLE II. BIDIMENSIONAL IMPULSE RESPONSE

Frame /Time Data /Frequency	5	6	7	8	9
1	-0.0009	0.0022	0.0008	0.003	-0.0009
2	-0.1074-j0.0021	0.0003-j0.2506	0.3202+j0.0019	-0.0012+j0.2497	-0.1074-j0.0011
3	-0.0018-j0.0003	0.5033+j0.001	0.9988+j0.0031	0.5028+j0.0019	-0.0018
4	-0.1068-j0.0038	0+j0.2506	0 .317+j0.0007	0.0019-j0.2504	-0.1068-j0.0045
5	-0.0005-j0.0002	0.0014-j0.0002	-0.0009-j0.0013	0.001-j0.0007	-0.0004

In order to estimate the accuracy of the realization two verifications have been performed.

- *Impulse response verification*

To obtain the impulse response 8 initial frames (becoming 16 after the OQAM modulation in the transmitter) are treated in the transmitter, then in the receiver. All frames contain zeros, except the fifth frame whose third data value is 1.

Table II presents the bidimensional impulse response of the filter bank multicarrier modem.

Data in Table II correspond to the theoretical OQAM response witch is presented in Table III.

TABLE III. THEORETICAL OQAM RESPONSE

Frame /Time Data /Frequency	6	7	8
2	-0.25j	0.32	0.25j
3	0.5	1	0.5
4	0.25j	0.32	-0.25j

- *Mean square error (MSE) estimation in a FBS-BFA loop with ideal channel*

A bipodal random sequence is generated at the transmitter input.. This sequence is compared with the sequence at the output of the receiver and the measured MSE is presented on figure 4. The average value of the MSE obtained is -50dB (theoretical worst case value –45dB).

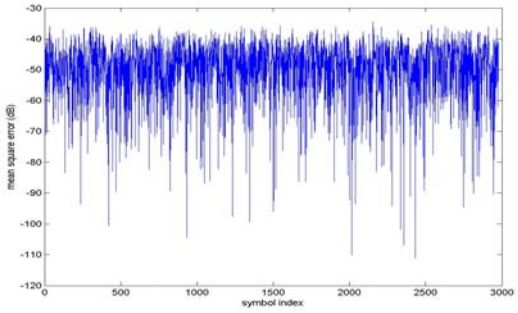


Figure 3. MSE estimation in a FBS-BFA loop with ideal channel

After hardware implementation a degradation of 4dB is measured.

CONCLUSION

This paper shows the feasibility of a Filter bank based multicarrier modem on FPGA. The proposed serial architecture for 256 subcarriers can be implemented into a FPGA XC2V1000 of Xilinx. The modem frequency is 7.46kHz per frame. The realization of additional IP cores in the modem as for example interpolator, decimator, equalizer and synchronization blocks will need an FPGA with 10 million gates. A higher modem frequency can be obtained by using parallel architecture for the realization.

ACKNOWLEDGMENT

The authors acknowledge the partial financial support from NATO grant PSL.CLG.977599/2005.

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